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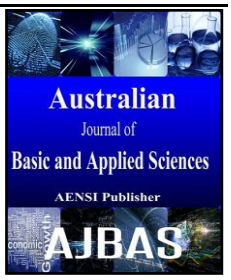


# High Speed Dct Architecture With Dadda Multiplier

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**ABSTRACT**

Discrete Cosine Transform (DCT) is Normally used for image/video compression technique.At past, DCT uses shift and add technique, main reason is multiplier occupies larger area when compared with adders. Later, due to emergence of scaling techniques, multiplier based architectures can be easily adopted for low-power and high speed applications ,to achieve this Tree based multipliers is used, which efficiently reduces the partial products by column compression technique. In the proposed work, Conventional DCT algorithm used to reduce the amount of multiplication involved, with that Dadda multiplier is designed and implemented in DCT architecture. In order to achieve high speed architecture the proposed algorithm can be used, because it requires only fewer multiplication.



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## INTRODUCTION

Image compression is very important for efficient transmission and storage of images. Need for communication of multimedia data through the network and accessing the multimedia data through Internet is growing rapidly, one of the efficient image compression technique is Discrete Cosine Transform (DCT)[8],where it is a lossy compression technique used in the image processing applications majorly in image and video compression.

DCT separates images into parts of different frequencies where less important frequencies are discarded through quantization and important frequencies are used to retrieve the image during decompression. Compared to other transforms, DCT has many advantages: (1) It has been implemented in linear circuits,(2) It has the ability to pack more information in less coefficients,(3) It minimizes the block appearance that results when boundaries between sub images become visible due to Technology scaling has driven out the area factor and paved a step for more performance. Due to technology scaling, area were not a constraint and the era of DCT presently concentrates on the high speed and low power DCT architecture.

Multipliers are used in a wide range of devices, from large scale processors to small embedded DSP chips. As multipliers are large, slow and complex components are used and a lot of research has been done to make the components smaller and faster. The two most important methods used is to either perform multiplication operation will be shift and add operations or add a multiplier unit.Multipliers in digital design are often divided into two subgroups: Array multipliers and tree multipliers. Array multipliers use a rigid pattern to construct their multipliers. This leads to compact designs and an evenly distributed delay. Tree multipliers on the other hand reduces the number of bits in each level in the tree until the calculation is done. Since this produces a complex tree structure, the delay is not evenly distributed. This may cause glitches that uses power. And the tree structure uses a lot of interconnection, end therefore it uses a lot more area. Despite the larger area and not so evenly distributed delay, the tree multipliers use less power than array multipliers. Another advantage tree multiplier have,is that their operation is lot faster when compared with array multipliers. The depth of an array multiplier is O(n)= n while it is O(n)=log2n for tree multiplier.Even though the wiring cause more delay for tree multiplier still perform faster than array multipliers.

### *Tree Multipliers:*

Tree multipliers mainly focus to reduce the partial products involves in the operation and it uses Column compression technique for reducing the Partial products(PP) by using half adders(HA) and

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full adders(FA) and the final row addition is done by Carry Save adders or Carry select adders. The Wallace algorithm (Anju, S., M. Saravanan, 2013)is the oldest of the algorithms which reduces the input matrix values by grouping the rows together, and performs reductions on each group where as the Dadda algorithm (Anju, S., M. Saravanan, 2013) reduces the tree by reducing columns instead of rows. The main aim of the algorithm is to reduce amount of elements as possible, Here Dadda multiplier requires only less amount of full adders and half adders when compared with Wallace multiplier.There are many advantages in using tree multipliers it actually used to reduce number of adders involved in partial products,As a result speed gets increased and Consumes less power.

***Dadda Multiplier:***

The Dadda algorithm shown in fig 1,reduces the partial products by reducing columns instead of rows. The aim of the algorithm is to use the less amount of elements as possible. To achieve this, the algorithm adds elements as late as possible. The algorithm is as follows (Samundiswary, P., K. Anitha, 2013; Saro Ramya, S., 2013):

1. Let d1 = 2 and dj+1 = b3·dj/2c, where dj is the maximum length of the tree at the j-the reduction stage. Find the largest j, so that at least one of the columns has more bits than dj.
2. Use FAs(FullAdders) and HAs(HalfAdders) to reduce the partial products, so that no column has more than dj bits left (see Figure 1)
3. If one or more columns contains more than two rows then j = j −1 and repeat step 2.

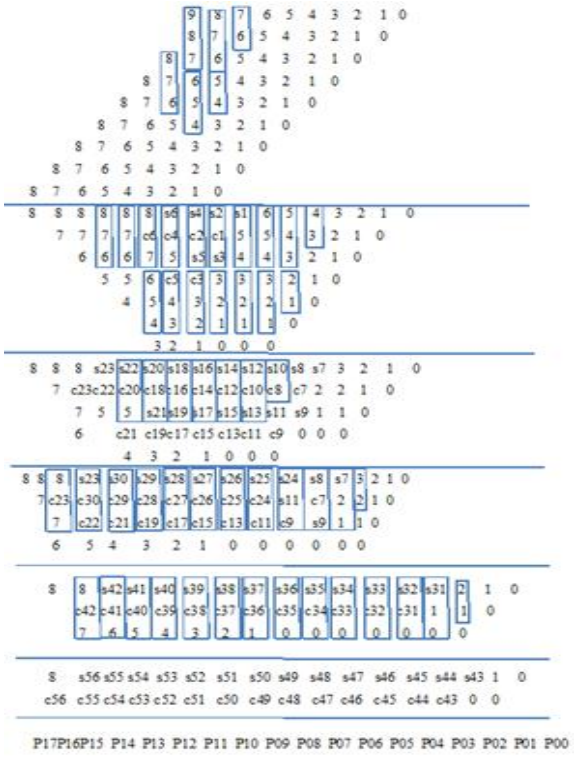


**Fig. 1:** Dadda multiplier architecture.

Dadda multiplier uses less FAs(Full Adders) and HAs(Half adders) than Wallace, it uses only minimum amount of FAs. Dadda algorithms uses less HAs(Half adders), but they would require more FAs. And since it allocates elements as late as possible.This is because the least significant bit would not get reduces until the last stage, and we will always start at bit two for the VMA. Therefore the VMA would always need (n*m)−2 bits for a Dadda multiplier. But the Dadda multiplier uses a lot less HAs, and found to be faster and smaller than the Wallace tree, despite the larger VMA(**vector merging adder)**.

For Dadda multipliers the number of full adders and half adders required always depends on the value of N.

Number of Full Adders used = $N^2$-4N+3

Number of Half Adders used = N-1

**Table I:** Number Of Adders Used In 9x9 Dadda Multiplier.

| Dadda multiplier | Number of adder used |
|---|---|
| Full Adder | 42 |
| Half Adder | 8 |

In the above TABLE I it shows the number of adders which have been involved in 9x9 multiplier.

***Conventional Dct Algorithm:***

The basic equation of the Discrete cosine transform algorithm described by following Eq.(1):

$$X(k) = e(k)\sum_{n=0}^{N-1} x(n)\cos\left[\frac{(2n+1)\pi k}{2N}\right], k = 0,1,\dots..,N-1 \quad (1)$$

The algorithmic architecture transformation (Ahmed, N., 1974), of this basic equation,. Consider algorithm transformation of 8-point DCT in Eq.(2),

$$X(k) = e(k)\sum_{n=0}^{7} x(n)\cos\left[\frac{(2n+1)\pi k}{16}\right], k = 0,1,..,7 \quad (2)$$

Where e(k) is the constant and takes the values of

$$e(k) = \begin{cases} \frac{1}{\sqrt{2}}, if\ k = 0 \\ 1, \quad otherwise \end{cases} \quad (3)$$

where the normal dct algorithm (Keshab, K., Parhi, 2007) requires N(N-1) multiplication[ie) if N=8 then it requires 56 multiplication ] Normally when multiplier gets increases it will normally affect the speed of the operation.

$$\begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \\ X(4) \\ X(5) \\ X(6) \\ X(7) \end{bmatrix} = \begin{bmatrix} C4 & C4 & C4 & C4 & C4 & C4 & C4 & C4 \\ C1 & C3 & C5 & C7 & -C7 & -C5 & -C3 & -C1 \\ C2 & C6 & -C6 & -C2 & -C2 & -C6 & C6 & C2 \\ C3 & -C7 & -C1 & -C5 & C5 & C1 & C7 & -C3 \\ C4 & -C4 & -C4 & C4 & C4 & -C4 & -C4 & C4 \\ C5 & -C1 & C7 & C3 & -C3 & -C7 & C1 & -C5 \\ C6 & -C2 & C2 & -C6 & -C6 & C2 & -C2 & C6 \\ C7 & -C5 & C3 & -C1 & C1 & -C3 & C5 & -C7 \end{bmatrix} \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \\ x(4) \\ x(5) \\ x(6) \\ x(7) \end{bmatrix} \quad (4)$$

Then the 8-point DCT shown in equation (4) can be rewritten as,

$X(1) = M_0C1 + M_1C7 + M_2C3 + M_3C5$
$X(7) = M_0C7 - M_1C1 - M_2C5 + M_3C3$
$X(3) = M_0C3 - M_1C5 - M_2C7 - M_3C7$
$X(5) = M_0C5 + M_1C3 - M_2C1 + M_3C7$
$X(2) = M_{10}C2 + M_{11}C6$
$X(6) = M_{10}C6 - M_{11}C2$
$X(4) = M_{100}C4$
$X(0) = P_{100}C4$

Where,

$M_0 = x0 - x7$ $\quad P_0 = x0 + x7$
$M_1 = x3 - x4$ $\quad P_1 = x3 + x4$
$M_2 = x1 - x6$ $\quad P_2 = x1 + x6$
$M_3 = x2 - x5$ $\quad P_3 = x2 + x5$
$M_{10} = P_0 - P_1$ $\quad P_{10} = P_0 + P_1$
$M_{11} = P_2 - P_3$ $\quad P_{11} = P_2 + P_3$
$M_{100} = P_{10} - P_{11}$ $\quad P_{100} = P_{10} + P_{11}$

where the values of $C_n$ can be calculated using the formula $c_n = \cos n\pi/16$ . All the cosine values are precomputed and the values are stored in the register file.In the Conventional DCT algorithm,it requires 22 multiplication and 28 addition and it compared with normal DCT algorithm as shown in TABLE II.

By solving the above architecture it results in 1D-DCT in order to obtain 2D-DCT architecture same process has to be repeated again.

***Applications:***

The above proposed Architecture can be used for various high speed image processing applications, using the Conventional DCT algorithm wih Dadda multiplier, the high speed DCT architecture is designed and the results are compared with Normal DCT Algorithm and tabulated in VI. The above 2D-DCT architecture can be used in various image compression techniques which improves the speed of the operation due to number of multipliers and adders gets limited in the above DCT architecture while compared with Previous algorithms, thus the above architecture is used to improve the speed of the operation

***Performance Evaluations:***

DCT architecture is analyzed with the previous work and the results is tabulated in the below table.

***Dct Architecture Comparisions:***

2D-DCT architecture is designed using the proposed Dadda multiplier. The architecture is verified using 180 nm cadence NC LAUNCH tool and the analysis is carried out by 180 nm cadence ENCOUNTER tool and the results were compared. The results obtained are shown in the TABLE II and III.

**Table II:** Comparisions Of Various 2d-Dct Architecture.

| Works | Multiplier Used | Adder Used(Add & Sub) |
|---|---|---|
| Conventional Dct Algorithm | 22 | 28 |
| Dct Algorithm | 56 | 64 |
| | | |

When compared with the proposed multipliers operate at the maximum frequency with low area and low power consumption. Our proposed multiplier based DCT architecture has 50% greater operating frequency which implies that the speed of the architecture is improved when compared to the Normal DCT algorithm shown in above TABLE II.

**Table III:** Area,Power And Delay Involved In Conventional Dct Architecture.

| Work | Area(μm^2) | Power(mw) | Delay(ns) |
|---|---|---|---|
| Conventional DCT Algorithm | 11664 | 1.95 | 8.8357 |

In above TABLE III shows about the Area, power and combinational delay requires in the Conventional dct architecture with Dadda multiplier.

***Conclusion:***

In this work to achieve high speed architecture, partial products is reduced effienciently with the help of Column compression technique used in Dadda Algorithm.While compared with other Tree multipliers Dadda multiplier requires only fewer amounts of full adders and half adders.Further this proposed Dadda multiplier is used in Conventional DCT architecture and finally ending up with the faster operation due to less multiplication and adders involved in the above DCT architecture,In future work the above proposed DCT architecture can be replaced by Fast 1-D DCT[2] algorithm which requires only 11 multiplication and Dadda multiplier can be replaced by vedic multiplier for the high speed applications.

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